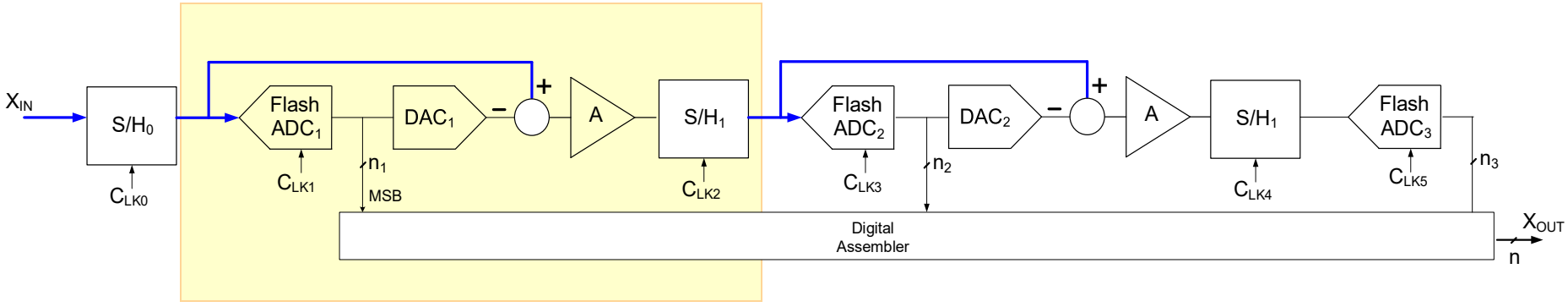
EE 435

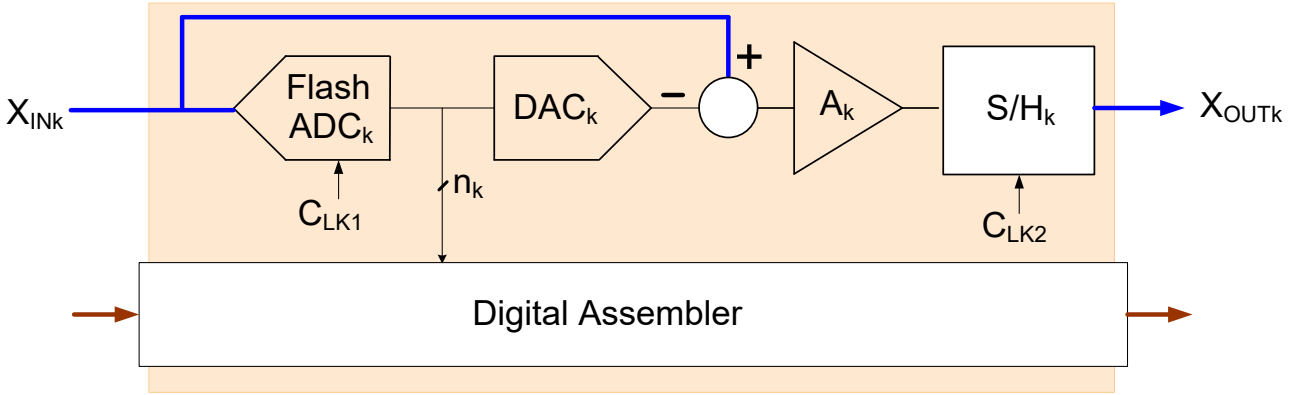
Lecture 38

ADC Design

Review from Last Lecture

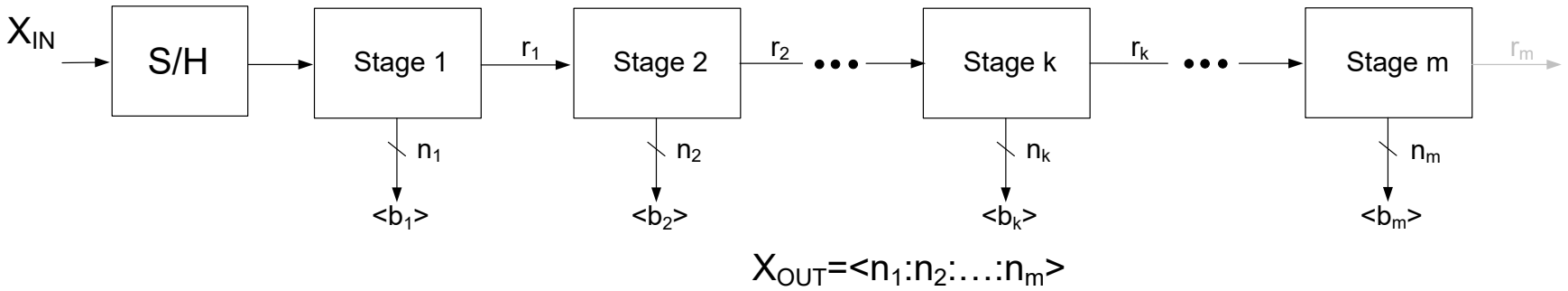
Three-Step Flash ADC with Interstage Gain





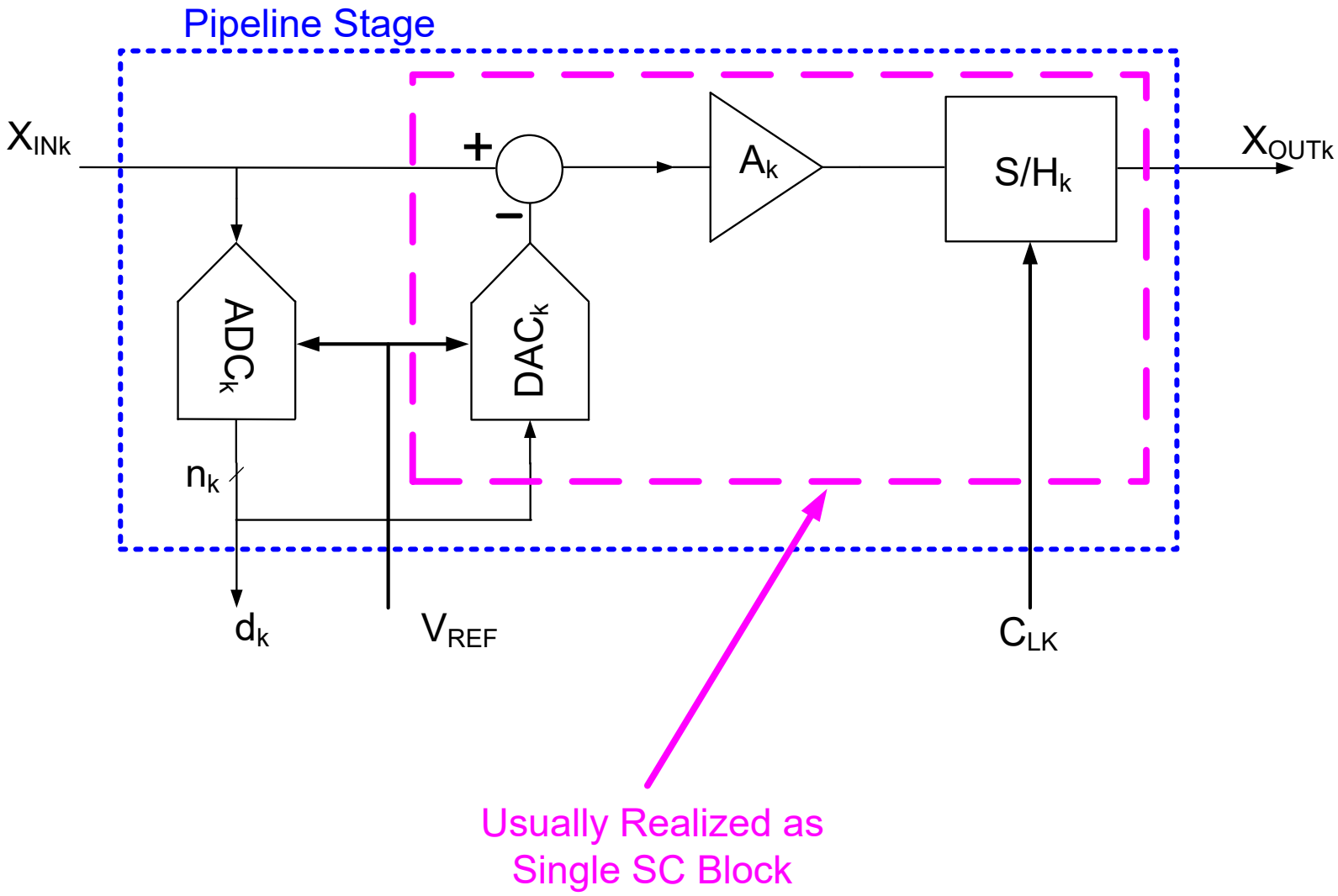
Review from Last Lecture

Pipelined ADC



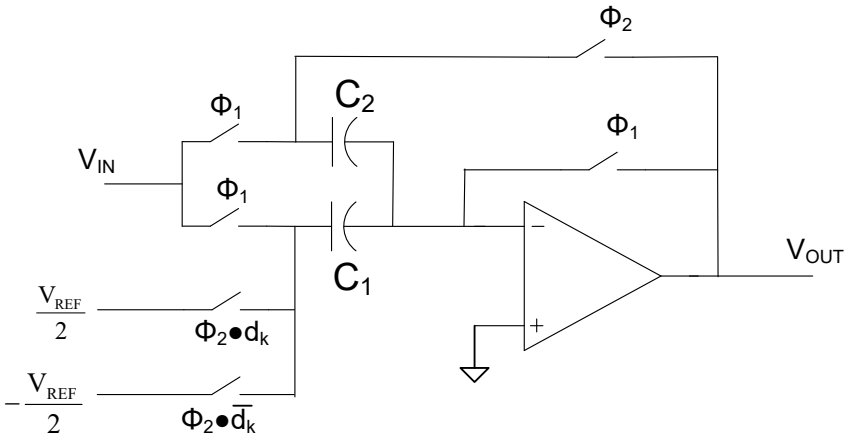
Review from Last Lecture

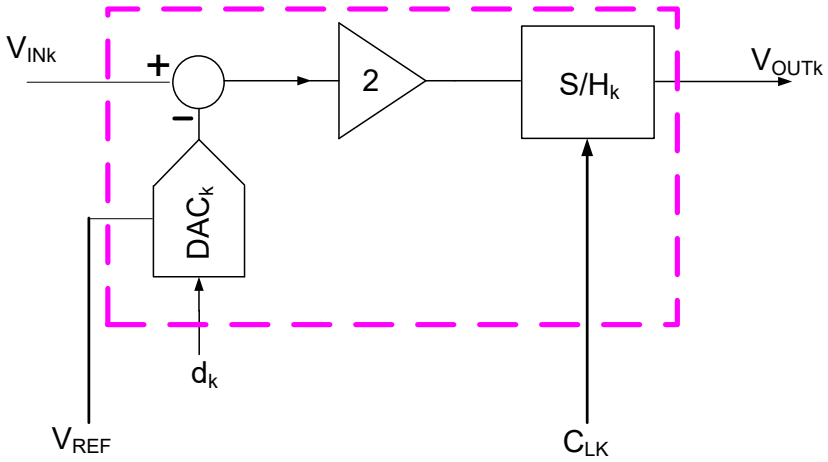
Pipelined ADC Stage k



Review from Last Lecture

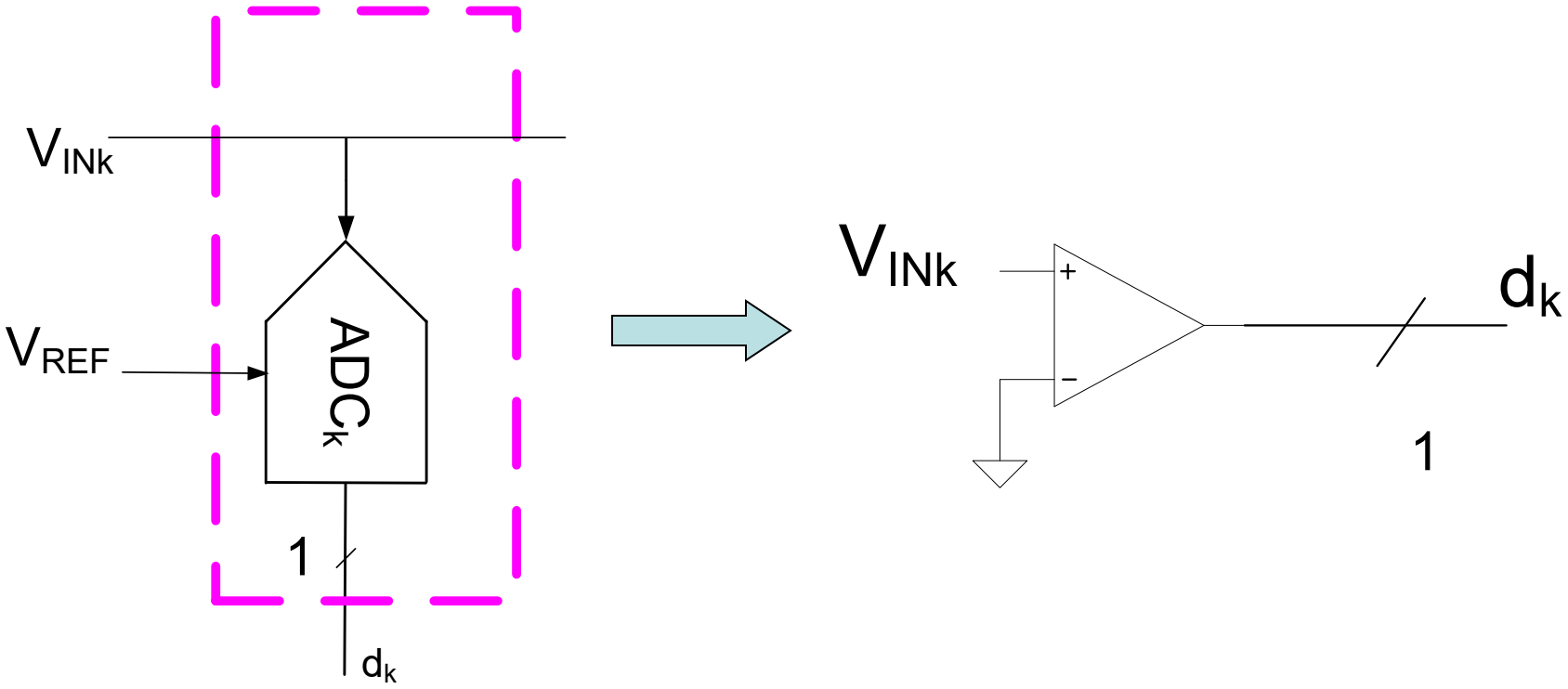
1-bit/Stage Pipeline Implementation





$$V_O = \begin{cases} 2V_{IN} + \dfrac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \dfrac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$

1-bit/Stage Pipeline Implementation



ADC Types

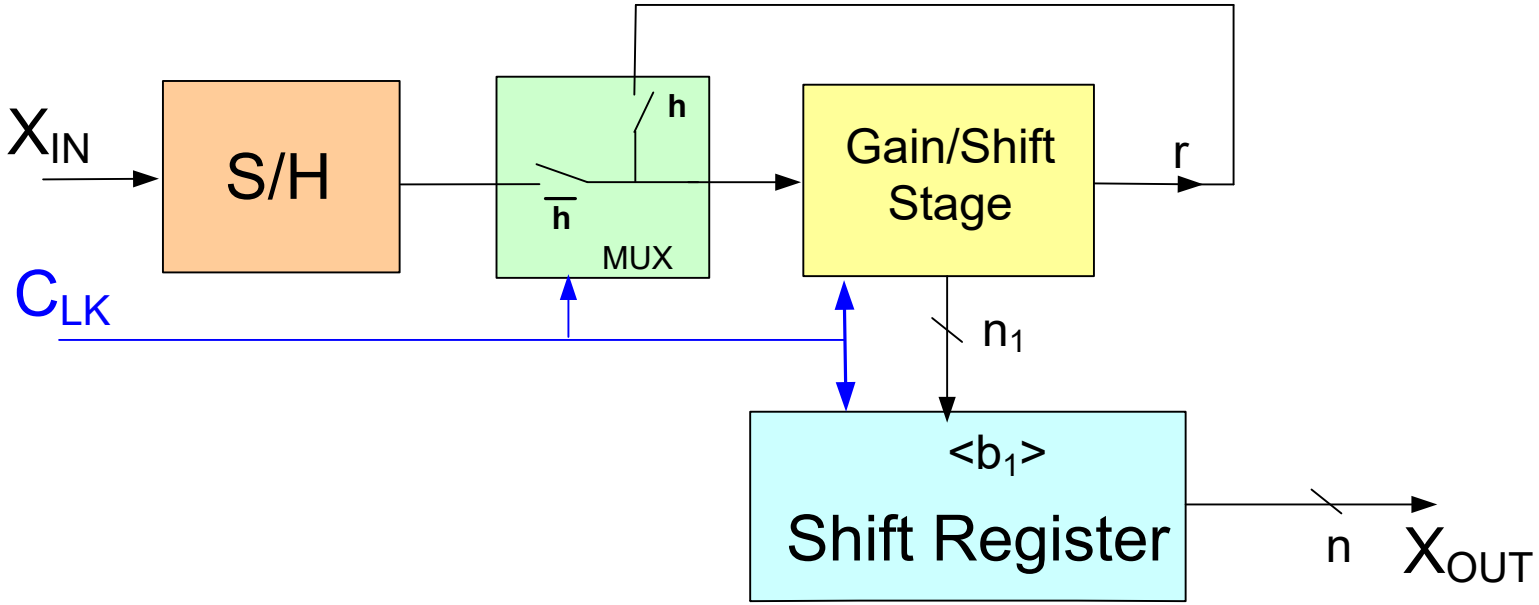
Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

Cyclic (Algorithmic) ADC



- Re-use Pipelined Stage
- Small amount of hardware
- Effective thru-put decreases

ADC Types

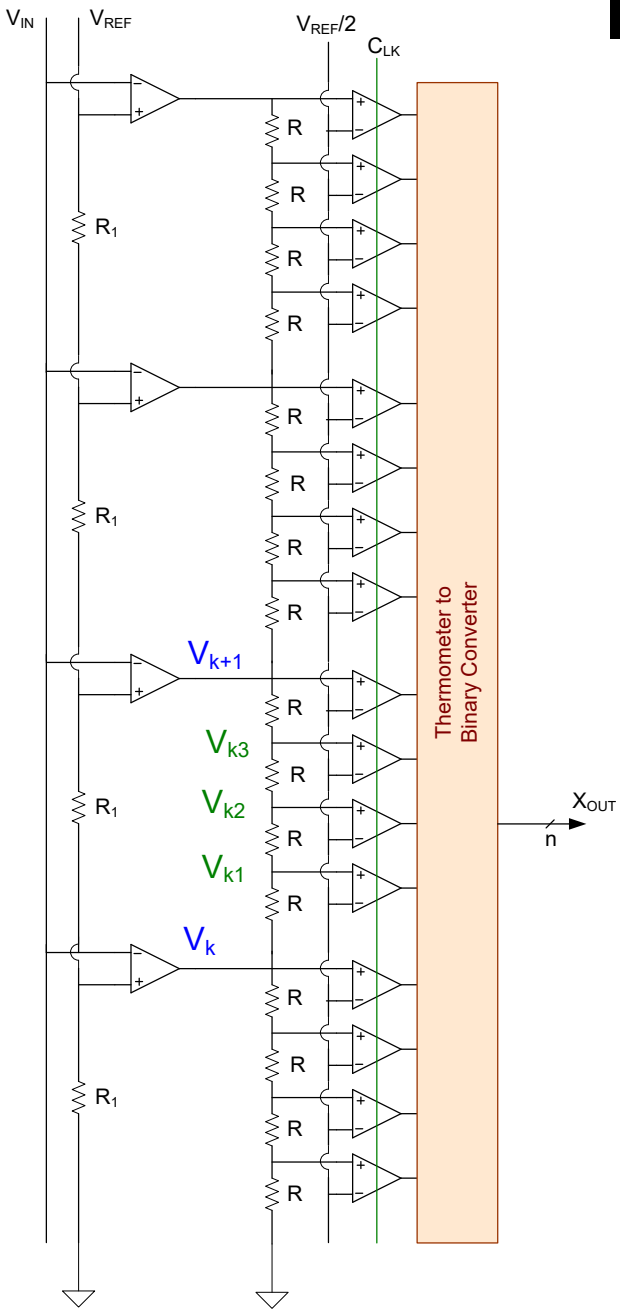
Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

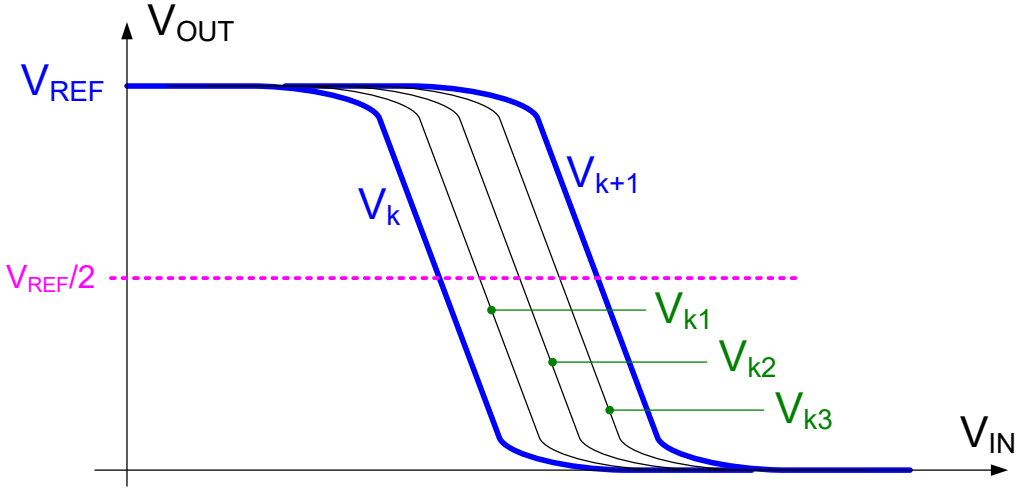
Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

Interpolating ADC



- Amplifiers are finite-gain saturating
- Shown for 4-bit
- Clocked comparators usually regenerative
- Reduces Offset Requirements for Comparators



ADC Types

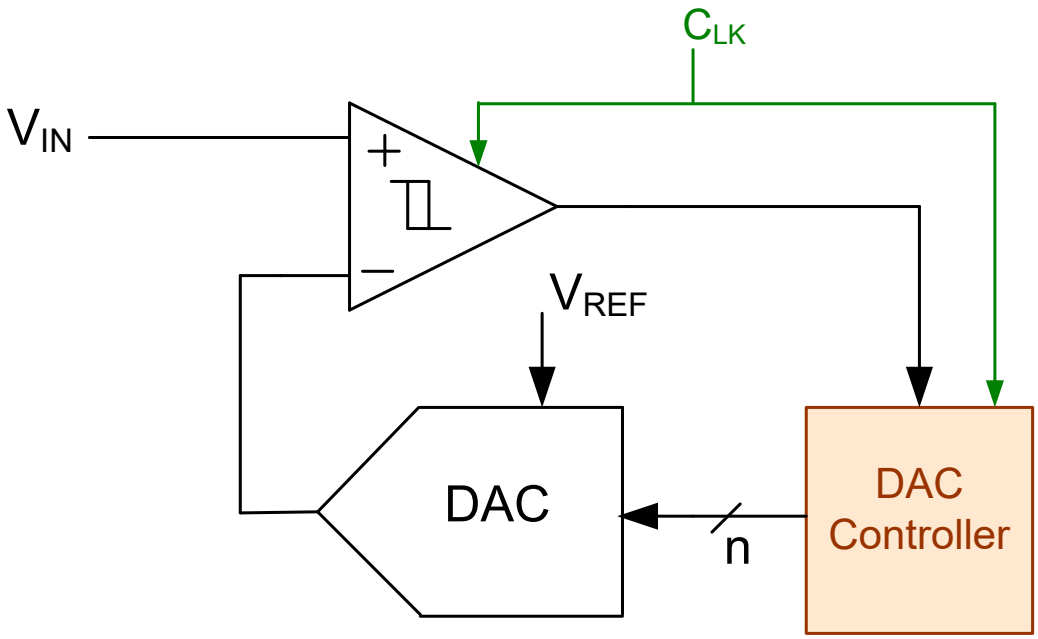
Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

SAR ADC



- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small

ADC Types

Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

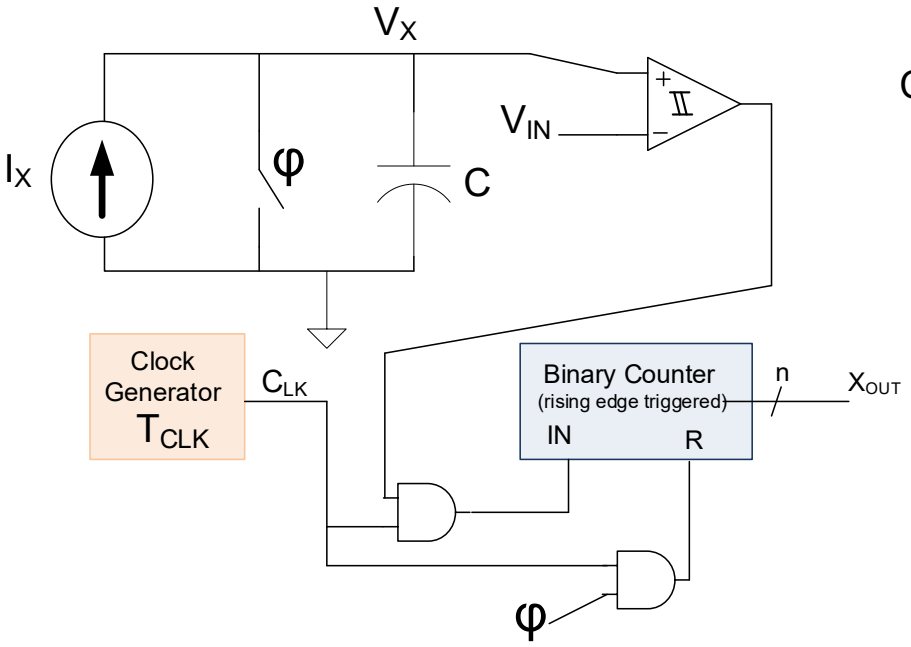
Over-Sampled

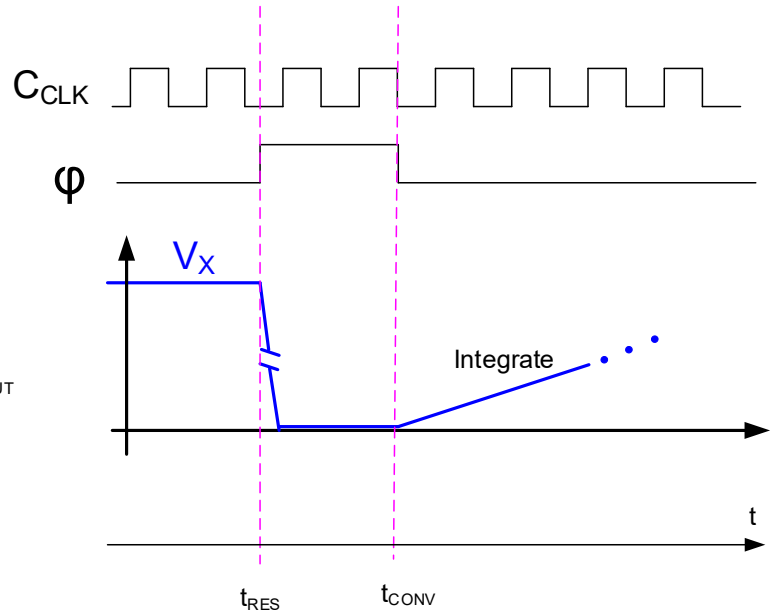
- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

And Single Slope

Single-Slope ADC

Sometimes Termed Integrating ADC





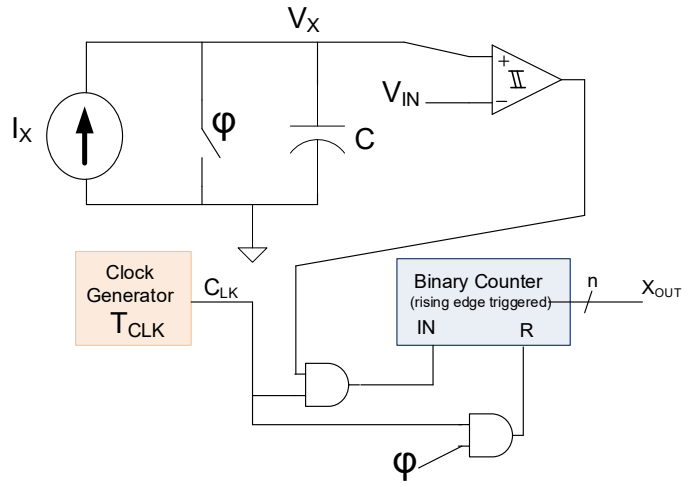
Falling edge of φ synchronous with respect to falling edge of C_{LK}

Can convert asynchronously wrt C_{CLK} or can be a clocked ADC where conversion clock signal is synchronous wrt C_{CLK}.

Output valid when comparator output goes low

Note V_{REF} not explicitly shown in ADC architecture

Single-Slope ADC



Operation:

Assume $V_X(t_{CONV})=0$

$$V_X(t) = \frac{1}{C}\int_{t_{CONV}}^{t} I_X dt = \frac{I_X}{C}(t - t_{CONV}) \qquad (1)$$

Assume $I_X, V_{REF}, R, C, T_{CLK}$ are selected to satisfy the relationship

$$V_{REF} = \frac{1}{C}\int_{t_{CONV}}^{t_{CONV}+2^n T_{CLK}} I_X dt = \frac{I_X}{C} 2^n T_{CLK} \qquad \text{thus} \qquad V_{LSB} = \frac{V_{REF}}{2^n} = \frac{I_X}{C} T_{CLK} \qquad (2)$$

Comparator will stop counter when $V_X=V_{IN}$ and counter output will be $X_{OUT}=k$

thus $V_X(t_{CONV} + kT_{CLK}) = V_{IN} + \varepsilon$ where $0<\varepsilon<V_{LSB}$

It follows from (1) that

$$V_X(t_{CONV} + kT_{CLK}) = \frac{I_X}{C} kT_{CLK} = V_{IN} + \varepsilon \qquad (3)$$

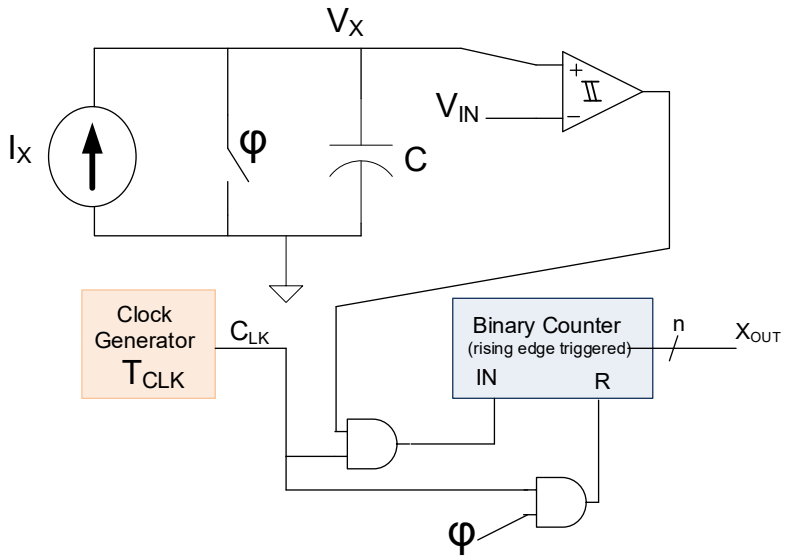
And finally from (2) and (3) that $V_{IN} = k\left(\frac{I_X}{C} T_{CLK}\right) - \varepsilon \cong \frac{k}{2^n} V_{REF}$

Single-Slope ADC

$I_X, V_{REF}, R, C, T_{CLK}$ must satisfy the relationship

$$V_{REF} = \frac{I_X}{C} 2^n T_{CLK} \qquad (1)$$

$$V_{IN} \cong \frac{k}{2^n} V_{REF}$$



Benefits: Very simple structure and can provide a low-cost easy solution for low speed applications

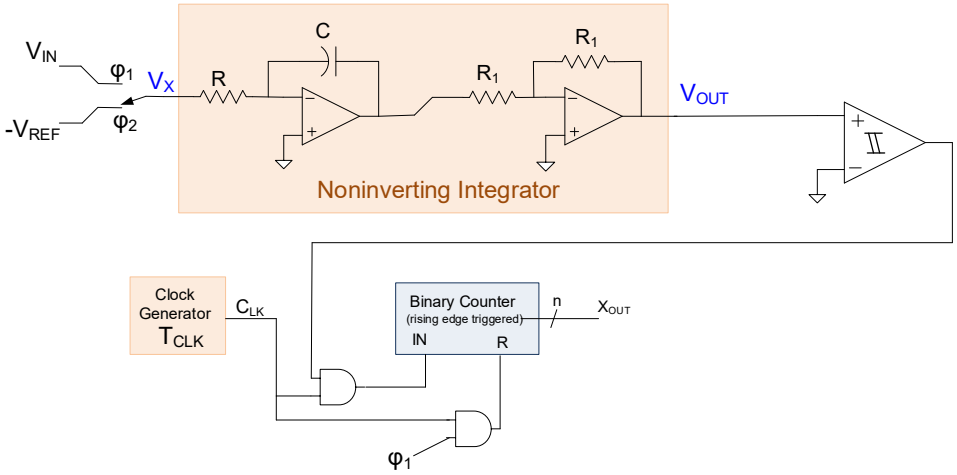
Limitations:

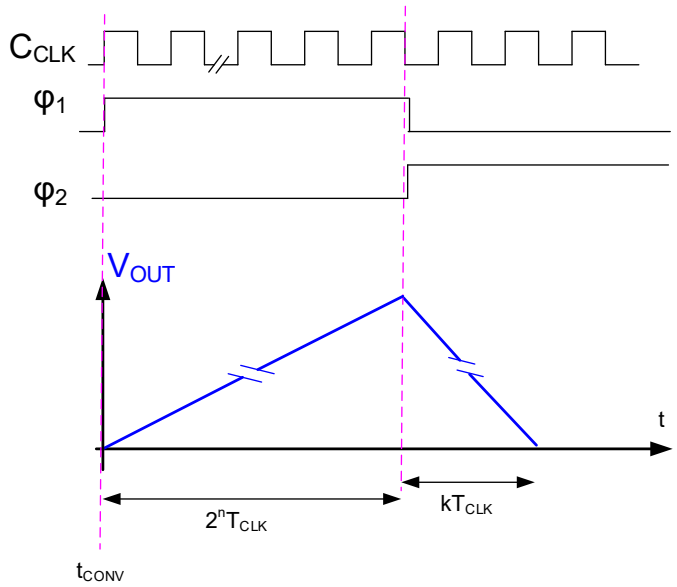
- Process variations make it difficult to satisfy (1)
- C is large and must be off chip
- Linearity of C important (since off-chip)
- Nonlinearity in I_X degrades performance
- R_{OUT} of I_X degrades performance
- Slow
- Not widely used

Options for improving performance:

- Introduce self-calibration cycle to satisfy (1) by trimming I_X or C
- Use high-impedance current source
- Use OP-Amp Based RC integrator

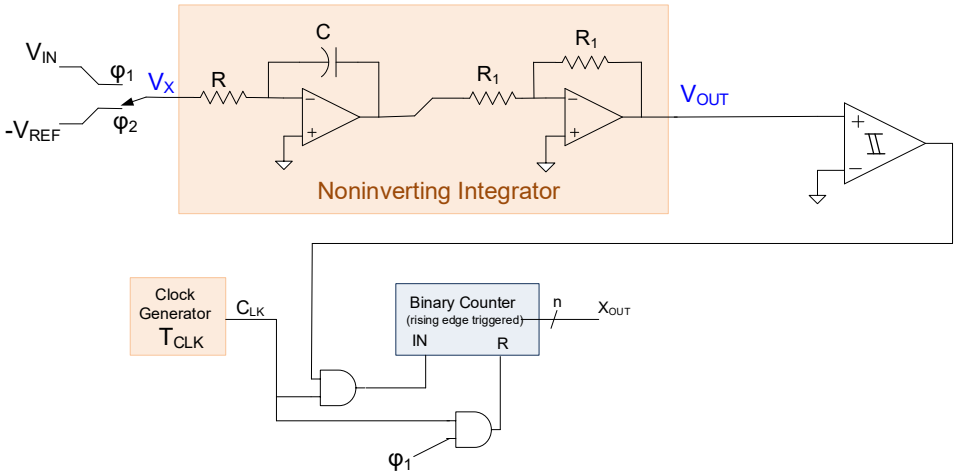
Dual-Slope ADC





- Output valid when comparator output transitions to Low
- Must set RC time constants and CCLK so output does not saturate
- Shown as noninverting integrator but slight modification will also work with inverting integrator
- Other integrator structures could be used
- Can leave one or more clock cycles between integrate up and integrate down

Dual-Slope ADC



Operation:

$$V_{OUT}(t) = \frac{1}{RC}\int_{t_{CONV}}^{t} V_X dt$$

During φ_1, integrate V_{IN} for time $2^n T_{CLK}$

At end of integrate up interval, $$V_{OUT}\left(2^n T_{CLK}\right) = \frac{1}{RC} V_{IN} 2^n T_{CLK}$$

Reset counter at time $2^n T_{CLK}$

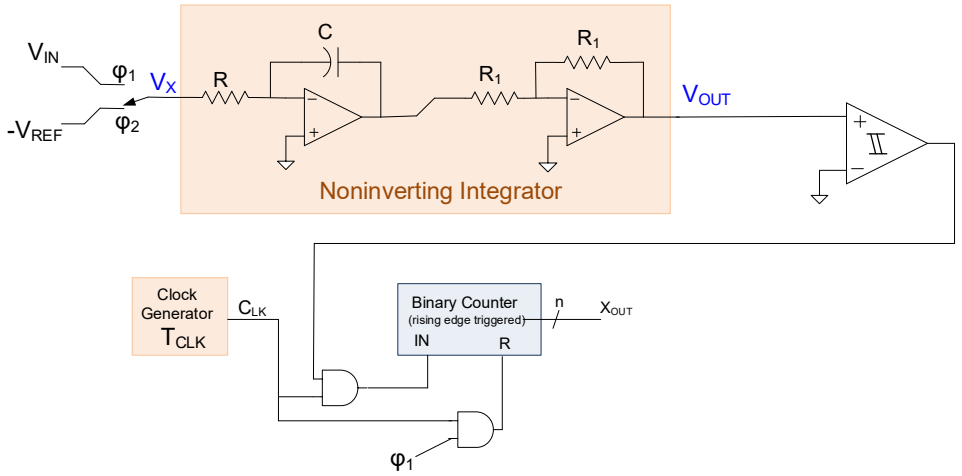
During φ_2, integrate $-V_{IN}$ until comparator goes low and count clock transitions during down integration interval. At time comparator changes states, $V_{OUT}=0$ and code in counter is k

$$0 = \frac{1}{RC}\int_{t_{CONV}}^{t_{CONV}+2^n T_{CLK}} V_{IN} dt - \frac{1}{RC}\int_{t_{CONV}+2^n T_{CLK}}^{t_{CONV}+2^n T_{CLK}+kT^{CLK}} V_{REF} dt \quad \Rightarrow \quad \frac{1}{RC} V_{IN} 2^n T_{CLK} = \frac{1}{RC} V_{REF} k T_{CLK}$$

Solving, obtain: $$V_{IN} = \frac{k}{2^n} V_{REF}$$

Dual-Slope ADC

$$V_{IN} = \frac{k}{2^n} V_{REF}$$



Observations:

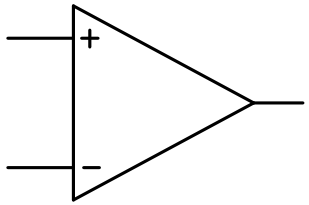
Benefits

- Not dependent upon R, C, or T_{CLK} (provided integrator does not saturate)
- Very simple structure that can give good results and cost can be low
- Inherently monotone

Limitations:

- Capacitor large and likely must be off-chip
- Linearity of capacitor is important (particularly of concern when off-chip)
- Slow
- Not widely used

Noise in ADCs and DACs

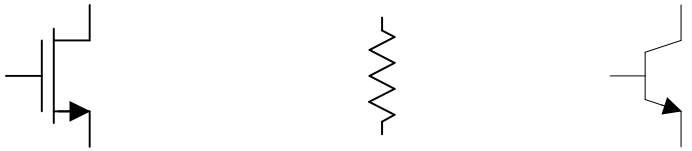


Noise in electronic devices and components introduce noise in electronic systems

Noise is of major concern in ADCs, DADs, and Op Amps

Beyond the scope of this course to go into lots of details about effects of device noise in these components but will provide a brief introduction

Devices that contribute noise :

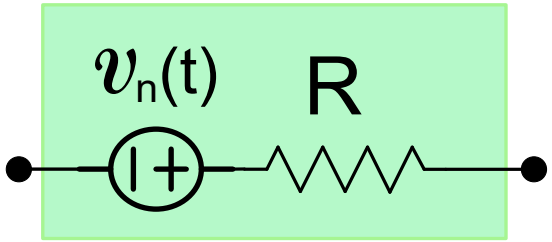


Capacitors and Inductors are noiseless:

Noise in DACs

Resistors and transistors contribute device noise but what about charge redistribution DACs ?

Noise in resistors:



Noise spectral density of $v_n(t)$ at all frequencies $S = 4kTR$

This is white noise !

k: Boltzmann's Constant
T: Temperature in Kelvin

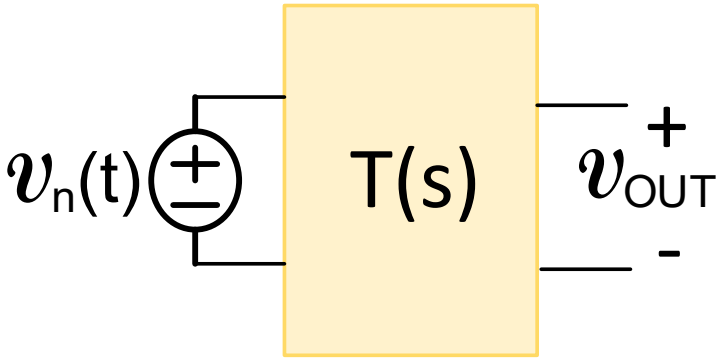
$k=1.38064852 \times 10^{-23}\ m^2\ kg\ s^{-2}\ K^{-1}$

At 300K, $kT=4.14 \times 10^{-21}$

Noise in DACs

Resistors and transistors contribute device noise but what about charge redistribution DACs ?

Noise in linear circuits:



$$v_{OUT_{RMS}} = \sqrt{\lim_{T\to\infty} \frac{1}{T} \int_{t=0}^{T} v_n^2(t)\,dt}$$

Difficult to obtain !

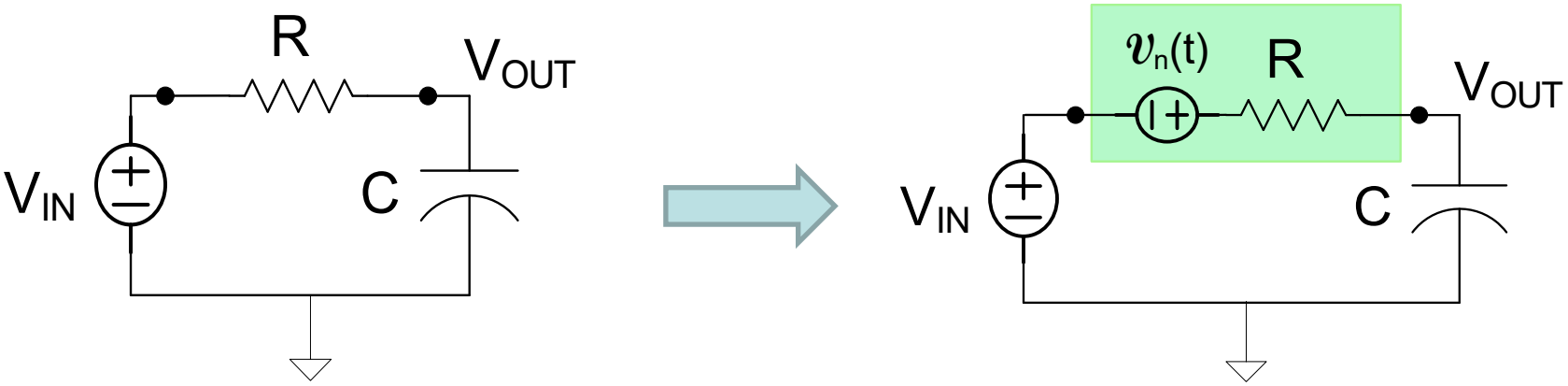
Due to any noise voltage source:

$$S_{V_{OUT}} = S_{V_n} \left| T_n(j\omega) \right|^2$$

Alternately and equivalently:

$$v_{OUT_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,df} = \sqrt{\int_{f=0}^{\infty} S_{V_n} \left| T_n(j\omega) \right|^2 df}$$

Example: First-Order RC Network

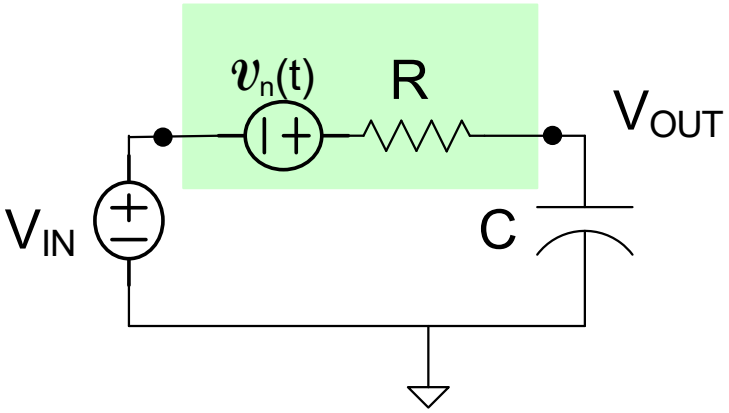


Noise transfer function: $T_n(s) = \frac{1}{1+RCs}$

$$S_{VOUT} = 4kTR\left(\frac{1}{1+(RC\omega)^2}\right)$$

$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{VOUT}\,df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\,df}$$

Example: First-Order RC Network

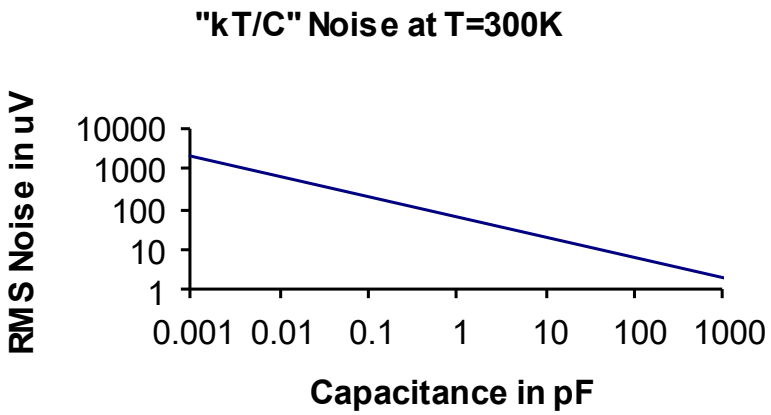


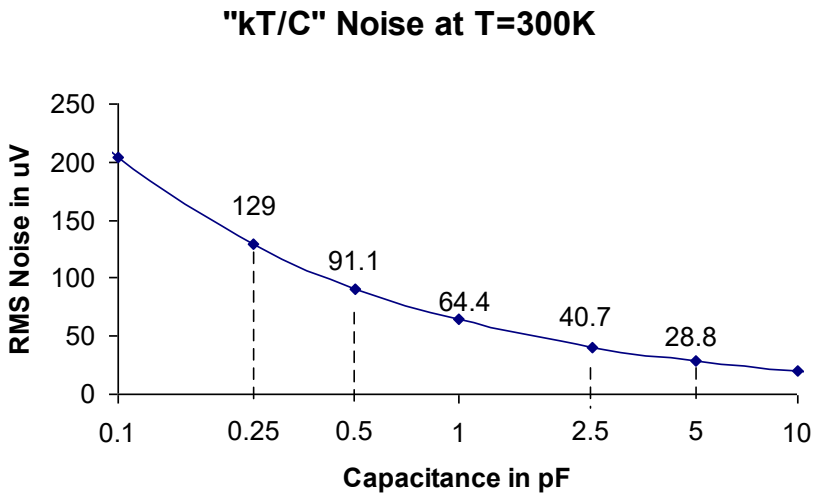
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\,df}$$

From a standard change of variable with a trig identity, it follows that

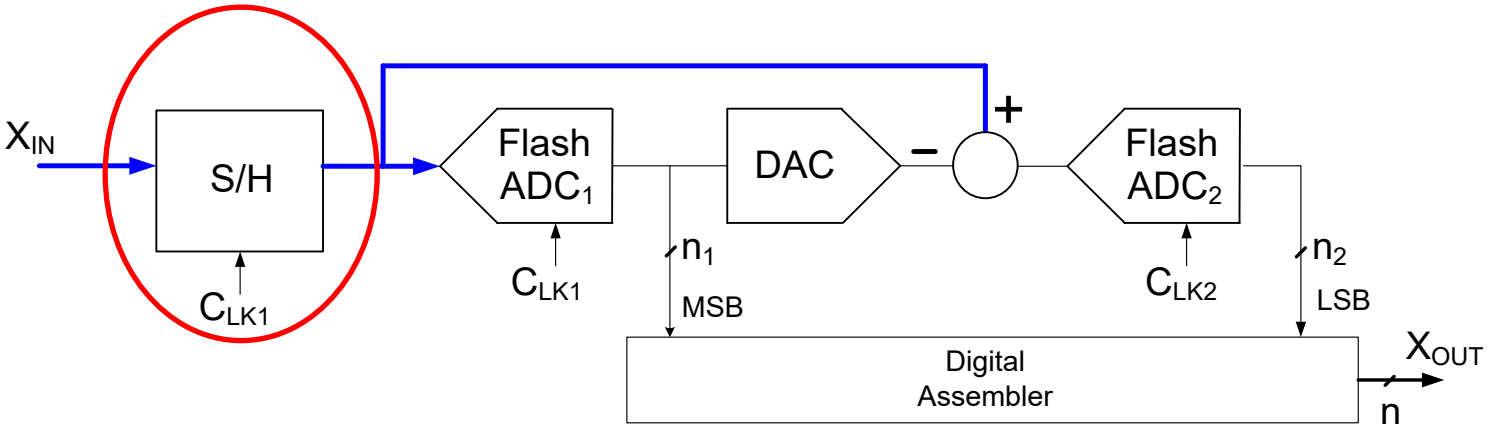
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,df} = \sqrt{\frac{kT}{C}}$$

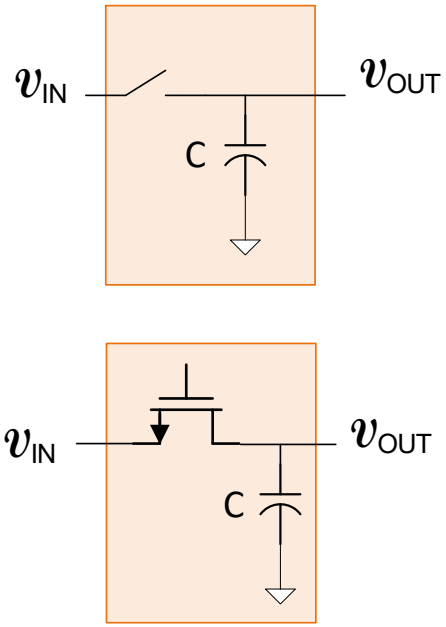
- The continuous-time noise voltage has an RMS value that is independent of R
- Noise contributed by the resistor is dependent only upon the capacitor value C
- This is often referred to at kT/C noise and it can be decreased at a given T only by increasing C


"kT/C" Noise at T=300K
RMS Noise in uV
10000
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Capacitance in pF


"kT/C" Noise at T=300K
RMS Noise in uV
250
200
150
100
50
0
129
91.1
64.4
40.7
28.8
0.1
0.25
0.5
1
2.5
5
10
Capacitance in pF

Sample and Hold Circuits





Basic S/H circuit

Slightly more complicated S/H used for input S/H

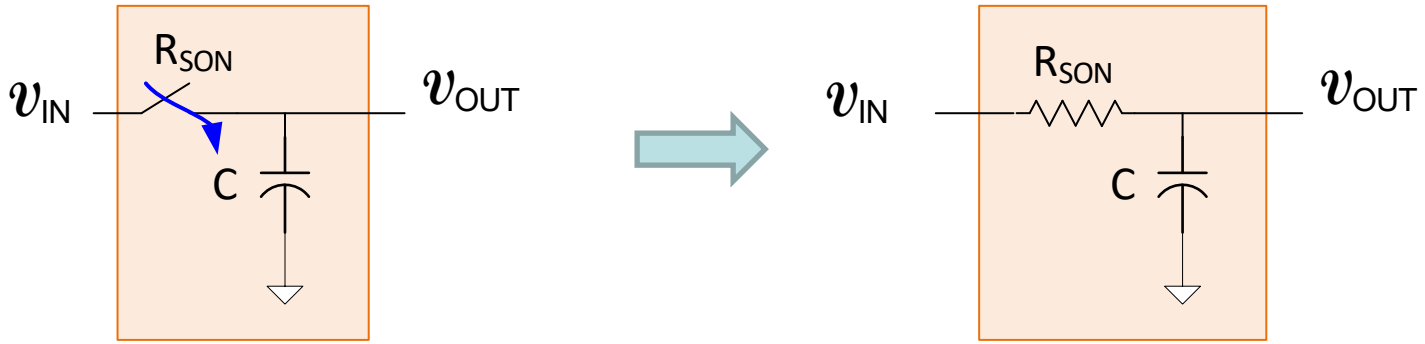
This simple structure used in some applications

Actually a Track and Hold Circuit

Noise characteristics of S/H similar to that of these simple samplers

Sample and Hold Circuits

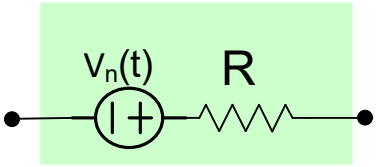
During Track Mode



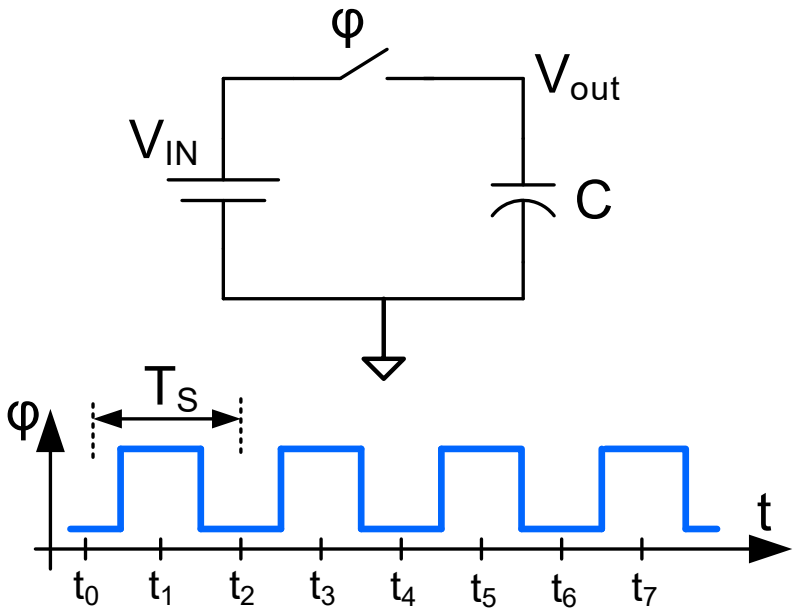
When switch is opened to take sample, noise on C is captured on C

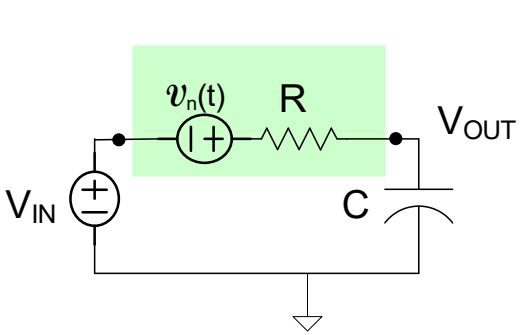
This noise becomes input noise to the ADC

Recall noise in resistor modeled as noise voltage source in series with R

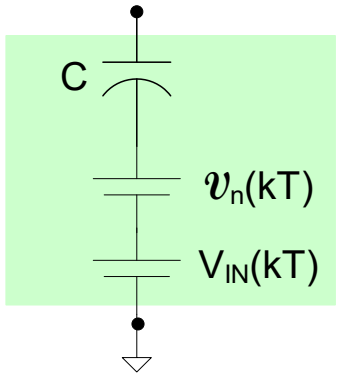


Sample and Hold Circuits





Track mode

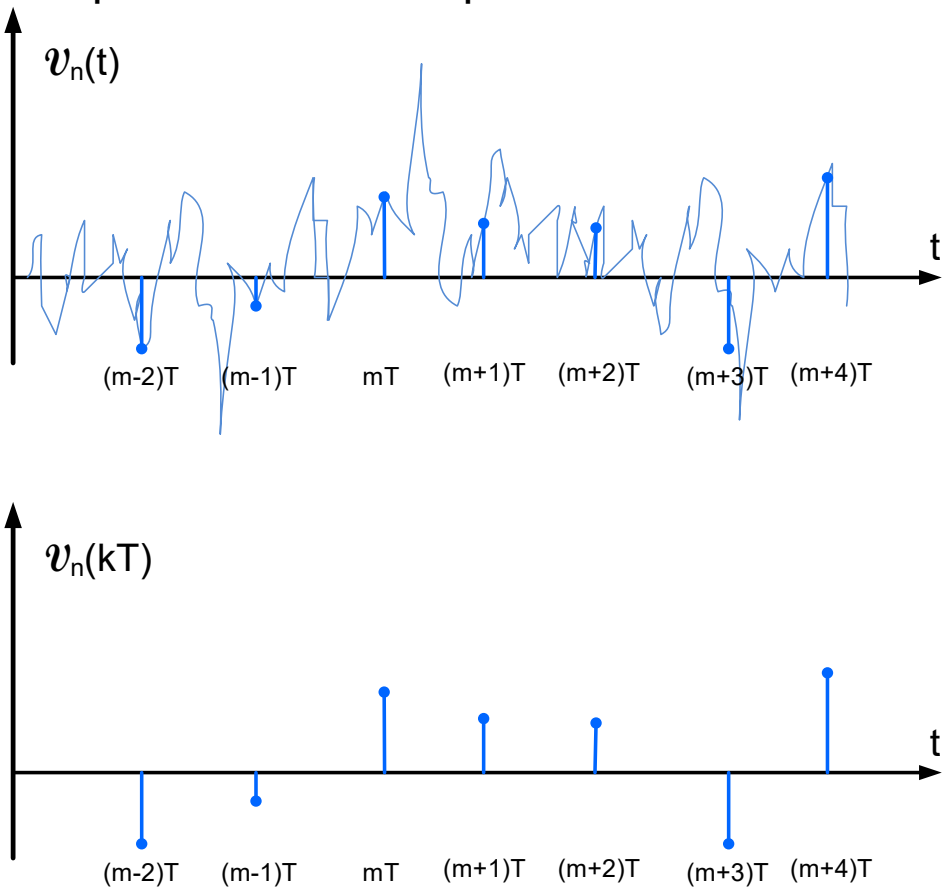


Hold mode

If switch opens fast, noise on C due to R is captured as $v_n(kT)$

Sample and Hold Circuits

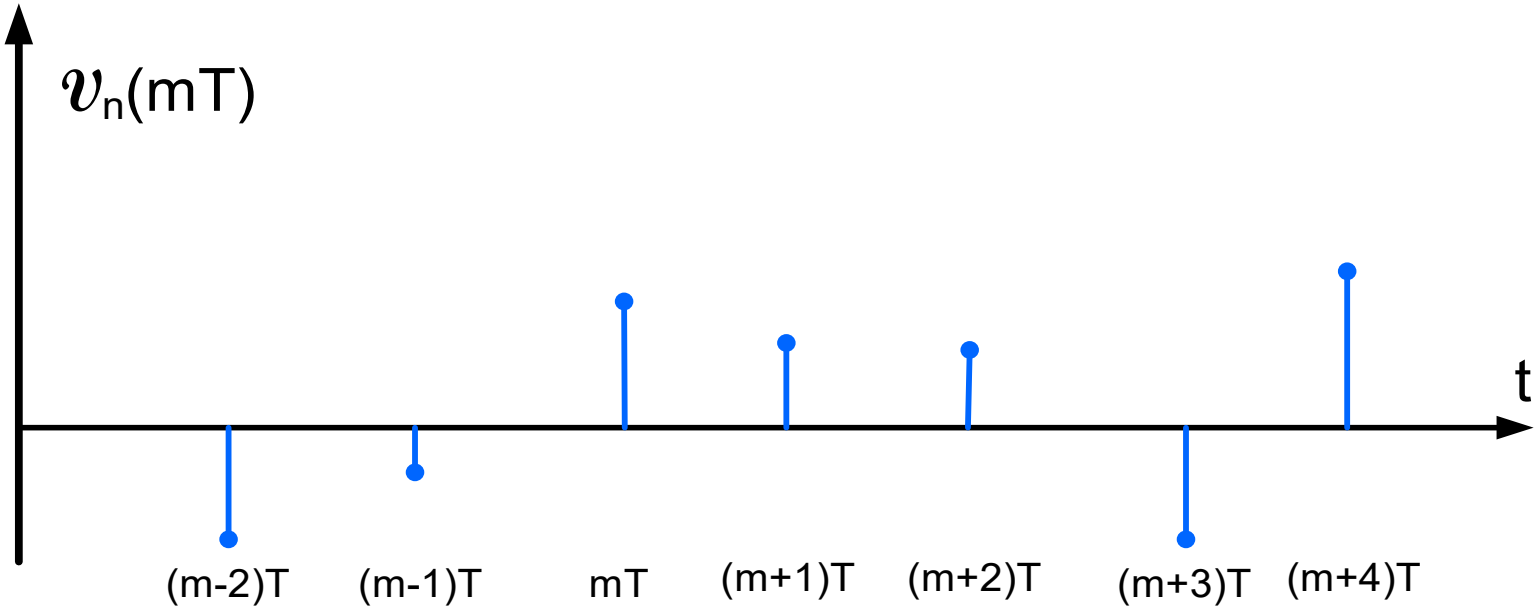
T is the period of the sampler



$v_n(mT)$ is a discrete-time sequence obtained by sampling continuous-time noise waveform

RMS value of noise input to pipelined ADC is that of the discrete time noise sequence

Sample and Hold Circuits



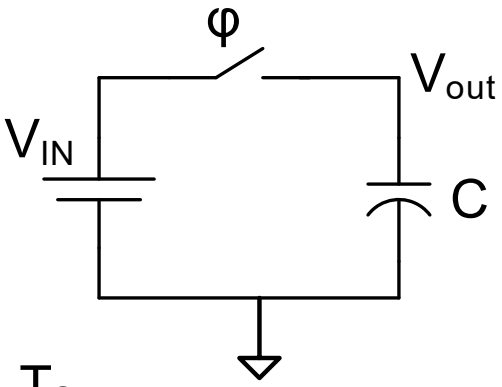
$$\hat{v}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{m=1}^{N} v^2(mT)\right)}\right) \underset{N\,large}{\simeq} \sqrt{\frac{1}{N}\sum_{m=1}^{N} v^2(mT)}$$

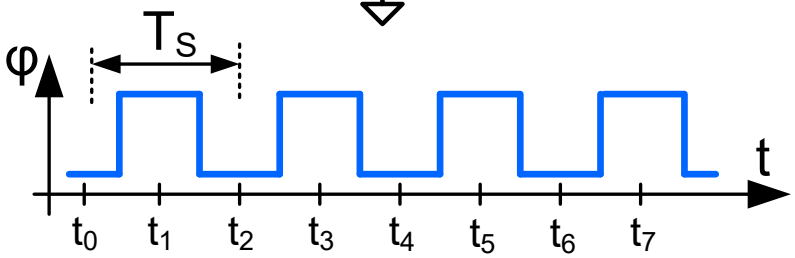
Theorem 1 If $v(t)$ is a continuous-time zero-mean noise source and $\langle v(kT) \rangle$ is a sampled version of $v(t)$ sampled at times T, 2T, …. then the RMS value of the continuous-time waveform is the same as that of the sampled version of the waveform. This can be expressed as $v_{RMS} = \hat{v}_{RMS}$

Theorem 2 If $v(t)$ is a continuous-time zero-mean noise signal and $\langle v(kT) \rangle$ is a sampled version of $v(t)$ sampled at times T, 2T, …. then the standard deviation of the random variable $v(kT)$, denoted as $\sigma_{\hat{v}}$ satisfies the expression $\sigma_{\hat{v}} = v_{RMS} = \hat{v}_{RMS}$

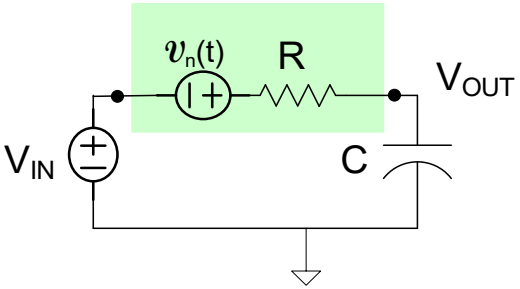
From Theorem 1 we obtain the RMS value of the switched capacitor sampler

Sample and Hold Circuits

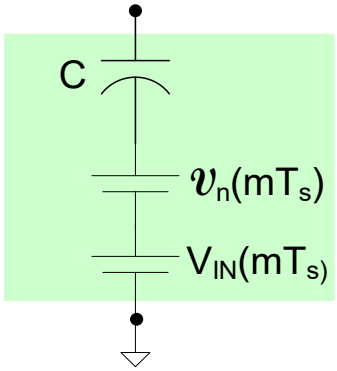




$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,df} = \sqrt{\frac{kT}{C}}$$



Track mode



Hold mode

$$v_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

k: Boltzmann's constant
T: temperature in Kelvin

RMS noise at output of basic SC S/H is independent of R but dependent upon C

Stay Safe and Stay Healthy !

End of Lecture 38